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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,918	07/09/2001	Ken Fernald	CYGL-24,692	7118
25883 7590 04/19/2007 HOWISON & ARNOTT, L.L.P. P.O. BOX 741715 DALLAS, TX 75374-1715			EXAMINER THAI, TUAN V	
			ART UNIT 2186	PAPER NUMBER
			MAIL DATE 04/19/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

**Notice of Allowability**  
**- SUPPLEMENTAL -**

Application No.

09/901,918

Examiner

Tuan V. Thai

Applicant(s)

FERNALD, KEN

Art Unit

2186

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Examiner interview conducted on April 04, 2007.
2. ☒ The allowed claim(s) is/are Original claims 1-3, 6-10 and 13-16 previously renumbered as 1-5, 7-11, 6 and 12 respectively.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
  1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material

5. ☐ Notice of Informal Patent Application

6. ☒ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_

7. ☒ Examiner's Amendment/Comment

8. ☐ Examiner's Statement of Reasons for Allowance

9. ☐ Other \_\_\_\_\_

**TUAN V. THAI**  
**PRIMARY EXAMINER**

*Group 2186*

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Attorney's Docket No.: CYGL-24,692

**IN THE UNITED STATES PATENT AND  
TRADEMARK OFFICE**

**In re application of:** Robert D. Norman      **Group:** 2186  
**Serial No.:** 09/901,918      **Examiner:** Tuan Thai  
**For:**      **METHOD AND APPARATUS FOR PROTECTING INTERNAL MEMORY  
FROM EXTERNAL ACCESS.**

**EXAMINER'S AMENDMENT**

1. An Examiner's Amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 C.F.R. 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the Issue Fee.

2. Authorization for this Examiner's Amendment was given in a telephone interview with Mr. Gregory M. Howison; Reg. No. 30,646 on April 04, 2007

3. The application has been amended as follows:

In the claims:

a. Please amend claims 1 and 8 as follows:

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**Claim 1.** (Thrice Amended) A method for protecting a memory space from external access, the memory space having a plurality of logical portions, comprising the steps of:

storing in a location in the memory space on one of the logical portions thereof a plurality of lock bits, each of the lock bits associated with a separate one of the logical portions of the memory space, including the logical portions in which the lock bits are stored, and determinative as to the access thereof for a predetermined memory access operation thereon, there being at least two different memory access operations;

detecting a request for access to a desired location in one of the logical portions in the memory space for operating thereon;

comparing the requested predetermined memory access operation with the one of the lock bits associated with the one of the logical portions to which the request for access is directed and determining if access is allowed thereto for the requested predetermined memory access operation of the at least two different memory access operations; and

[if allowed,] performing the requested predetermined memory access operation of the at least two different memory access operations on the desired location in the memory space; otherwise denying said access;

wherein the predetermined memory access operation includes

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an erase of the associated logical portion for an addressable location therein, and wherein location the plurality of lock bits comprises storing in a variable location in the memory space the plurality of lock bits and storing the location of the lock bits in a known location in the memory space, such that in the step of comparing, the location of the lock bits is first read from the known location in the memory space and then this read location is utilized to read the lock bits from the memory space.

**Claim 8.** (Thrice Amended) A method for protecting a memory space from an external access, the memory having a plurality of logical portions, comprising the steps of:

storing in a location in the memory space on one of the logical portions thereof a plurality of lock bits, each of the lock bits associated with a separate one of the logical portions of the memory space, including the logical portion in which the lock bits are stored, and determinative as to the access thereof for a predetermined memory access operation thereon;

detecting a request for access to a desired location in one of the logical portions in the memory space for operating thereon;

comparing the requested predetermined memory access operation with the one of the lock bits associated with the one of the logical portions to which the request for access is

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directed and determining if access is allowed thereto for the requested predetermined memory access operation; and

[if allowed,] performing the requested predetermined memory access operation on the desired location in the memory space;  
otherwise denying said access;

wherein the predetermined memory access operation includes an erase of the associated logical portion for an addressable location therein; and wherein the step of storing in a location the plurality of lock bits comprises storing in a variable location in the memory space the plurality of lock bits and storing the location of the lock bits in a known location in the memory space, such that in the step of comparing, the location of the lock bits is first read from the known location in the memory space and then this read location is utilized to read the lock bits from the memory space.

#### **REASONS FOR ALLOWANCE**

4. The following is an Examiner's Statement of Reasons for Allowance:

The prior arts of record do not teach nor suggest, *either alone or in combination*, all the limitations of the claimed invention (claims 1 and 8), particularly method for protecting a memory space from the external access as being claimed in the amended claims 1 and 8 of the current invention. The prior arts

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of record do not teach the comparing of the requested predetermined memory access operation with the lock bits associated with one of the logical portions to determine if memory access is allowed wherein the predetermined memory access operation includes an erase of the associated logical portion for an addressable location, and storing in a variable location in the memory space the plurality of lock bits and storing the location of the lock bits in a known location in the memory space such that the location of the lock bits is first read from the known location in the memory space, and the read location is utilized to read the lock bits from the memory space.

In light of the foregoing claims 1 and 8 of the present application are found to be patentable over the prior arts.

Claims 2-3, 6-7, 15, 9-10, 13-14 and 16 further limit the allowable independent claims. These claims are therefore allowable for the same reason as set forth above.

Any comments considered necessary by Applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V.

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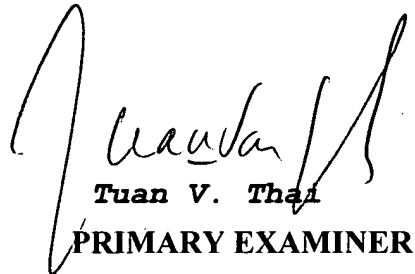
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Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**TVT**/April 04, 2007

  
**Tuan V. Thai**  
**PRIMARY EXAMINER**  
**Group 2100**